REMARKS

I. Introduction

At the time of the Office Action dated April 3, 2006, claims 1-16 were pending in this application. In this Amendment, claims 1, 3 and 6 have been amended, and claim 2 have been canceled. Care has been exercised to avoid the introduction of new matter. Claims 1, 3 and 6 have been amended to improve wording, and claims 1 and 6 have also been amended based on claim 2.

II. The Objection to the Specification

The Examiner has objected to the abstract because it includes two paragraphs. In response, the abstract has been amended to be in single paragraph format. Withdrawal of the objection to the specification is respectfully solicited.

III. The Objection to Claim 2

Claim 2 has been objected to because according to the Examiner, the recitation "a wiring length between the clock input terminal of the semiconductor chip and the area terminal is equal" is unclear. Applicants note that when claim 1 was amended to include the recitation of claim 2, the recitation was revised to address the Examiner's concern. Withdrawal of the objection to the claim 2 is, therefore, respectfully solicited.

IV. The Rejection of 1-6, 9, 11-12 and 15

Claims 1-6, 9, 11-12 and 15 have been rejected under 35 U.S.C. §102(b) as being unpatentable over Erdal et al. The Examiner asserted that Erdal et al. discloses a hierarchical clock distribution system identically corresponding to what is claimed.

Applicants submit that Erdal et al. does not disclose a clock delay adjusting method including all the limitations recited in independent claim 1, as amended. Specifically, the reference does not disclose, at minimum, "at least one of the hierarchical blocks has a plurality of area terminals, and the wiring length to the clock input terminal from one of the plurality of area terminals is equal to that from another area terminal," recited in claim 1 (originally recited in claim 2).

Erdal et al. discloses that "[t]he individual time delays provided by the delay buffers B are selected to equalize the clock delay between the driver 64 and clocked circuit elements or cells C in each block" (column 3, lines 55-60). However, Erdal et al. does not disclose that "at least one of the hierarchical blocks has a plurality of area terminals, and that the wiring length to the clock input terminal from one of the area terminals is equal to that from another area terminal," recited in claim 1. In rejecting claim 2, the Examiner asserted that Erdal et al. in column 3, lines 55-60 (see above) describes the "wiring length." However, it is apparent that Erdal et al. simply describes adjusting the time delays by delay buffers B, but does not disclose adjusting a clock delay by wiring length.

Independent claim 6 also recites, among other things, that a clock delay from the area terminal to each clock input circuit is adjusted based on wiring length from the clock input terminal to each area terminal. As set forth above, Erdal et al. does not teach adjusting the time delay based on the "wiring length."

Accordingly, Erdal et al. does not identically disclose a clock delay adjusting method including all the limitations recited in independent claims 1 and 6. Dependent claims 3-5, 9, 11, 12 and 15 are also patentably distinguishable over Erdal et al. at least because these claims include all the limitations recited in independent claims 1 and 6, respectively. Applicants, therefore, respectfully solicit withdrawal of the rejection of the claims under 35 U.S.C. §102(b) and favorable consideration thereof.

V. The Rejection of Claims 7, 8, 10, 14 and 16

Claims 7, 8, 10, 14 and 16 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Erdal et al. in view of Pileggi et al. Applicants submit that claims 7, 8, 10, 14 and 16 are patentably distinguishable over Erdal et al. and Pileggi et al. at least because the claims respectively include all the limitations recited in independent claims 1 and 6. It is noted that Pileggie does not cure the above-described deficiencies of Erdal et al.

Accordingly, Applicants respectfully solicit withdrawal of the rejection of the claims under 35 U.S.C. §103(a) and favorable consideration thereof.

VI. The Rejection of Claim 13

Claim 13 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Erdal et al. in view of Furuta et al. (U.S. Patent No. 5,978,930). Applicants submit that claim 13 is patentably distinguishable over Erdal et al. and Furuta et al. at least because the claim includes all the limitations recited in independent claim 1 or 6. It is noted that Furuta et al. does not cure the above-described deficiencies of Erdal et al.

Accordingly, Applicants respectfully solicit withdrawal of the rejection of the claims under 35 U.S.C. §103(a) and favorable consideration thereof.

VII. Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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